PVP 12

Code: EEPC2T5A

I M.Tech-II Semester–Regular/Supplementary Examinations – July 2017

DIGITAL CONTROL SYSTEMS
(POWER SYSTEM CONTROL AND AUTOMATION)

Duration: 3 hours Max. Marks: 70

Answer any FIVE questions. All questions carry equal marks

1. a) Explain the examples of data control systems of the following: 10 M
   i) A step motor control system
   ii) A digital computer controlled rolling mill regulating system

   b) Describe the frequency domain characteristics of the zero order hold. 4 M

2. a) Solve the following difference equation 7 M
   y (k+2)+3y(k+1)+2y(k)= 0 and y(-1)= -1/2, y(-2)=3/4

   b) Obtain the inverse z-transform of 7 M

   (i) $X(z) = \frac{z^{-2}}{(1 - z^{-1})^3}$ (ii) $X(z) = \frac{z+2}{z^2(z-2)}$

3. a) Explain the mapping between S-plane and Z-plane with primary strips and complementary strips. 7 M

b) A discrete time system x(k+1)=Ax(k) +Bu(k) has the system matrix $A = \begin{bmatrix} 1 & a \\ 2 & 1/2 \end{bmatrix}$.

For what value 'a' is the system stable? 7 M

4. a) Derive the steady state error conditions for step and ramp input. 7 M

b) Explain the design of the digital PID controller and PI controller in the Z-plane. 7 M

5. Obtain the state equation and output equation matrices for the system defined by $G(z) = \dfrac{0.17z + 0.04}{z^2 - 1.1z + 0.24}$ by using 14 M

a) Controllable canonical form

b) Observable canonical form

c) Jordon canonical form.

6. a) Derive the Ackermann's formula for the determination of the state feedback gain matrix. 7 M

b) Examine whether the discrete data system

$$x(k+1) = Ax(k) + Bu(k), \quad y(k) = Cx(k)$$

Where $A = \begin{bmatrix} 0 & -1 \\ 1 & -1 \end{bmatrix}$, $B = \begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix}$, $C = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$

Is (i) State controllable (ii) Observable. 7 M

7. a) Define the following terms: 6 M

   i) Full order state observer
   ii) Minimum order state observer
   iii) Reduced order observer.

b) Derive the error dynamics of the full order state observer. 8 M

8. Explain the architecture and features of TMS 320 Digital Signal Processor. 14 M